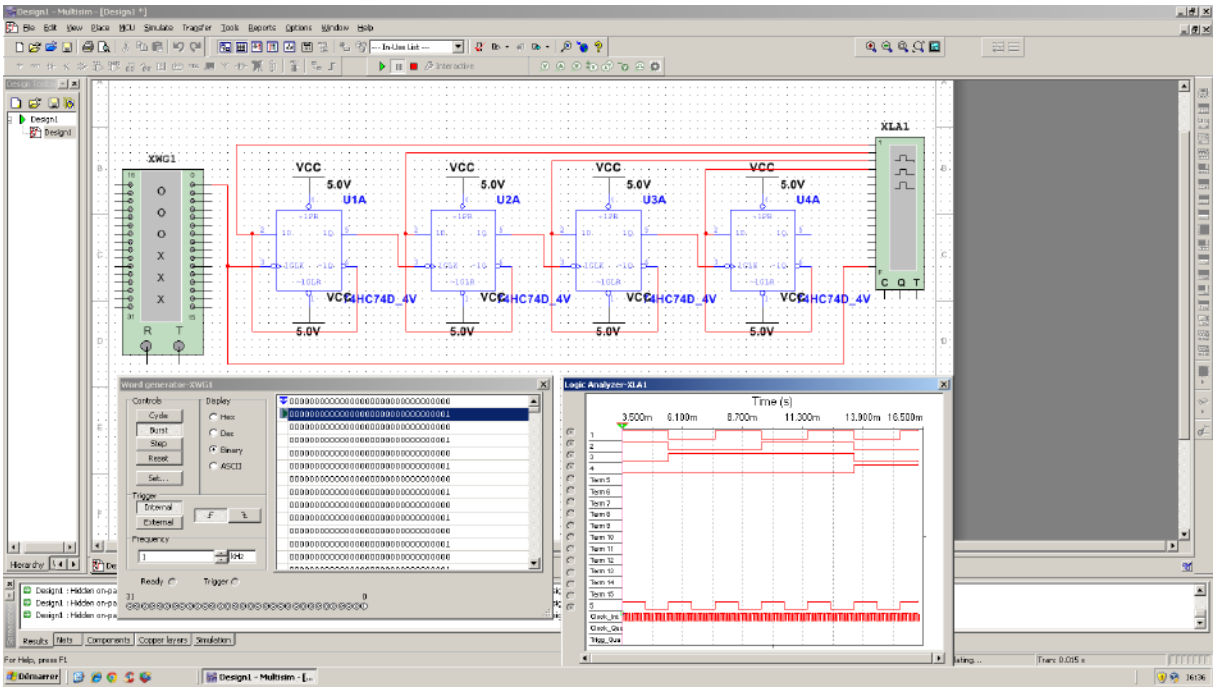
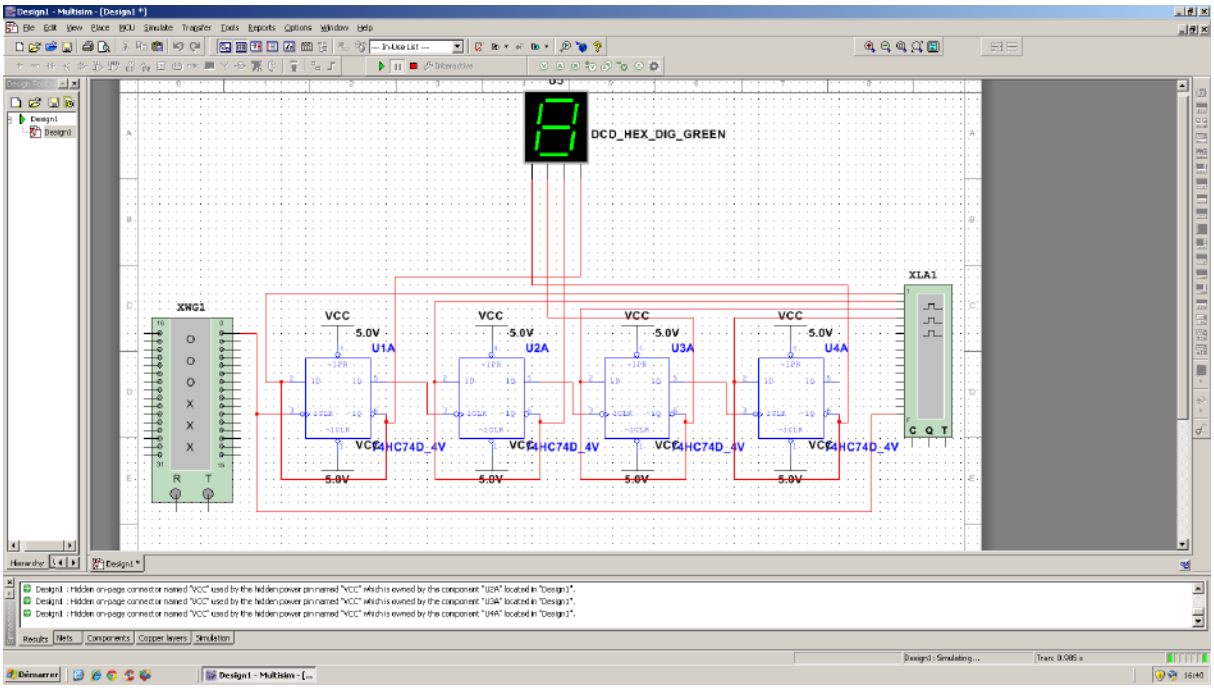
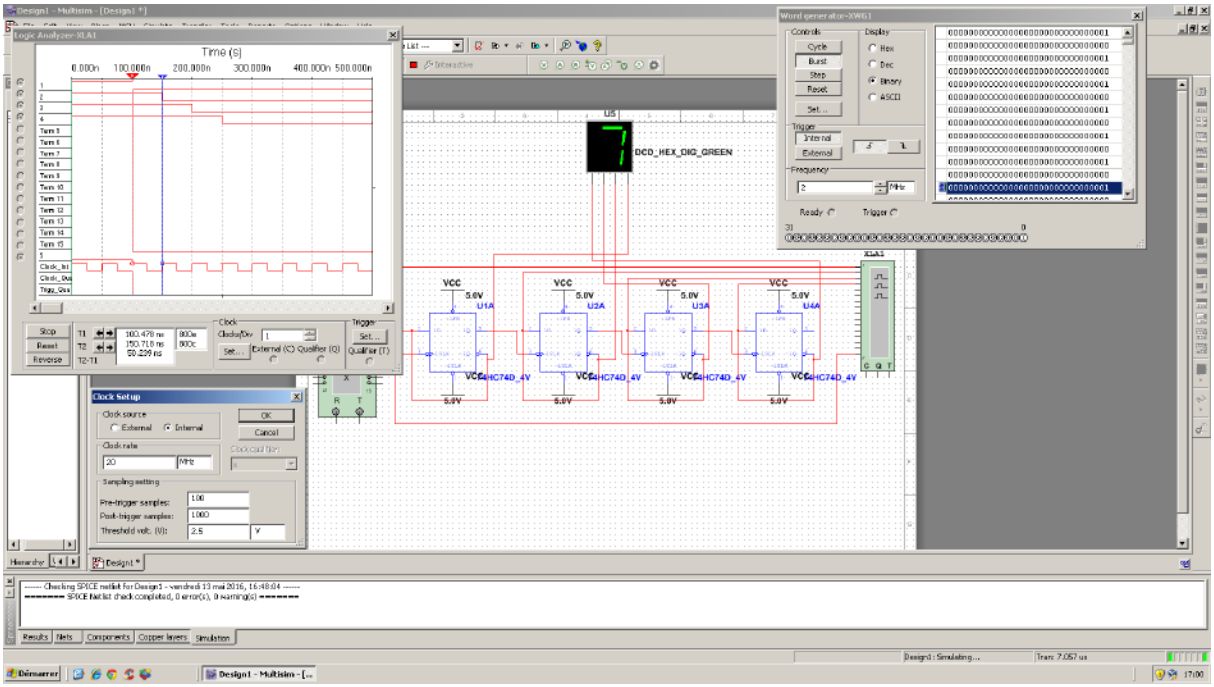
1.2)



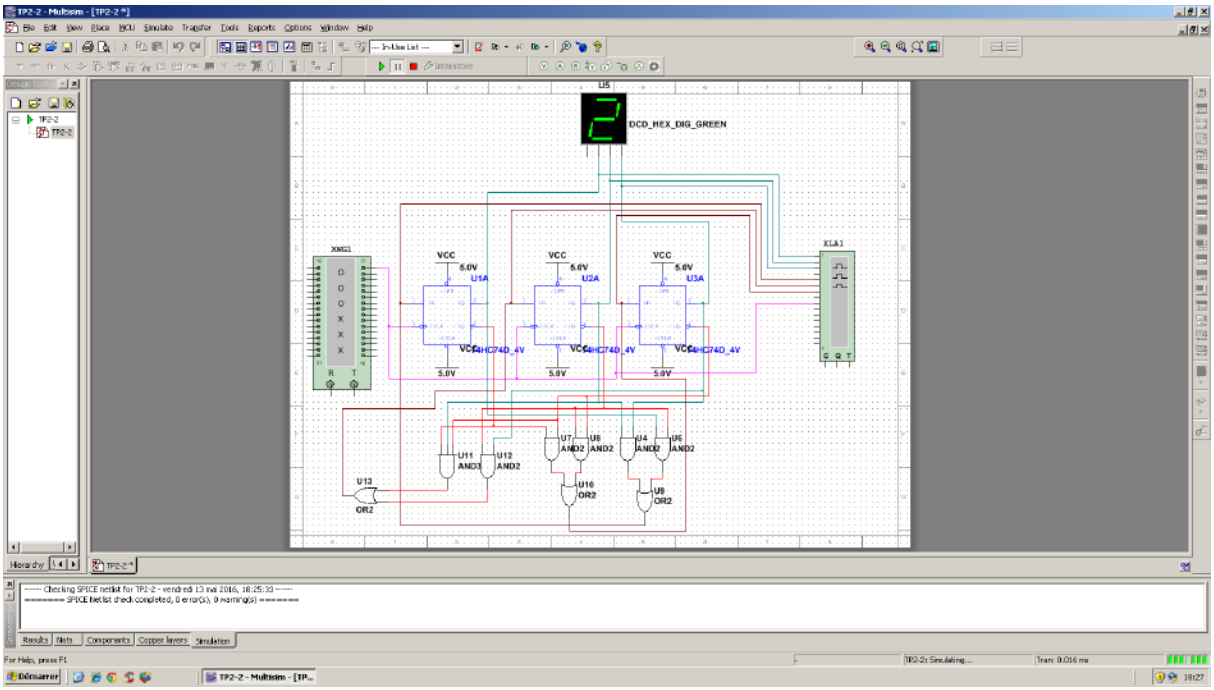
Avec afficheur :



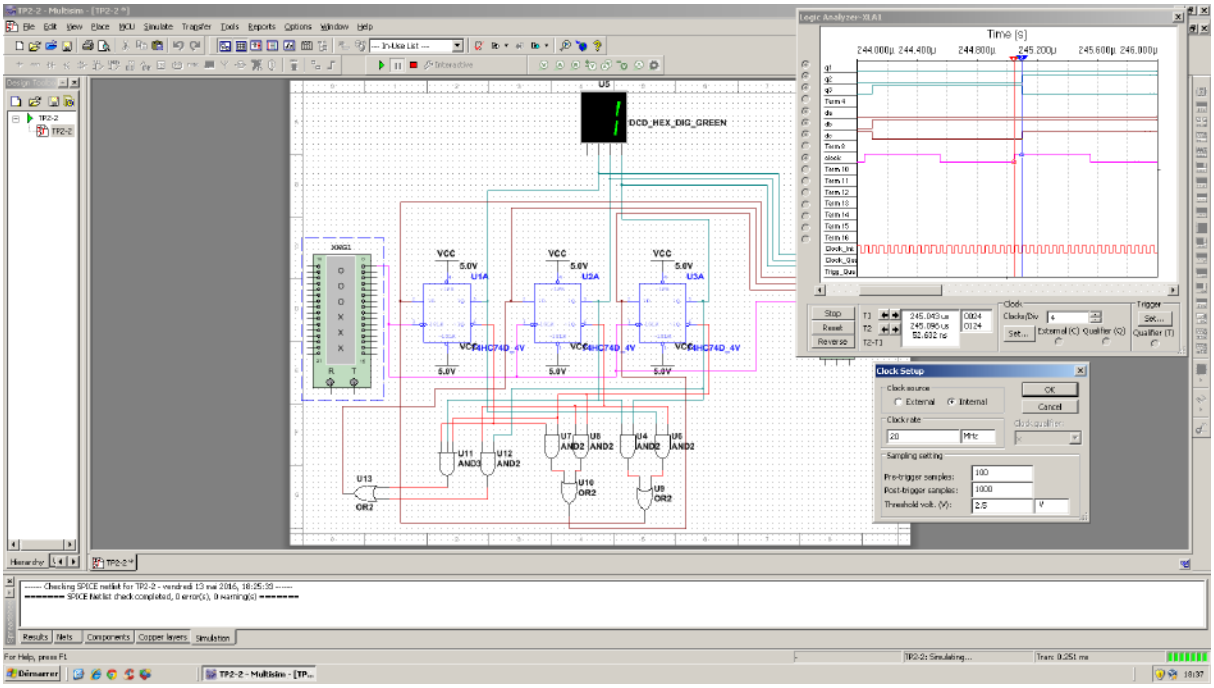
1.3)

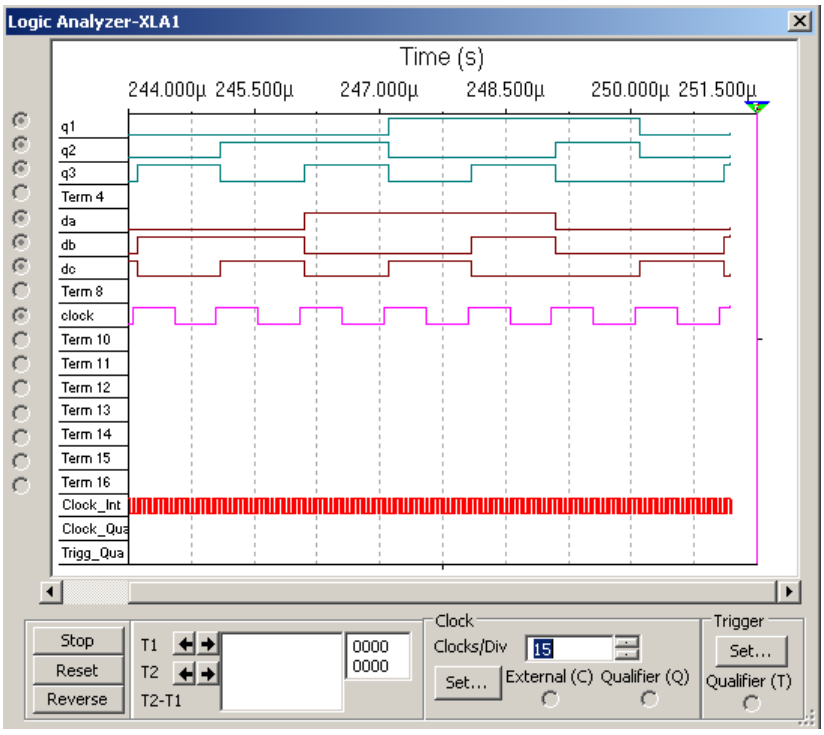

Logic Analyzer-XLA1
Time (s)
Word generator-XWG1
U5
DCD_HEX_DIG_GREEN
Clock Setup
VCC
5.0V
U1A
U2A
U3A
U4A
74HC74D_4V

2.2)

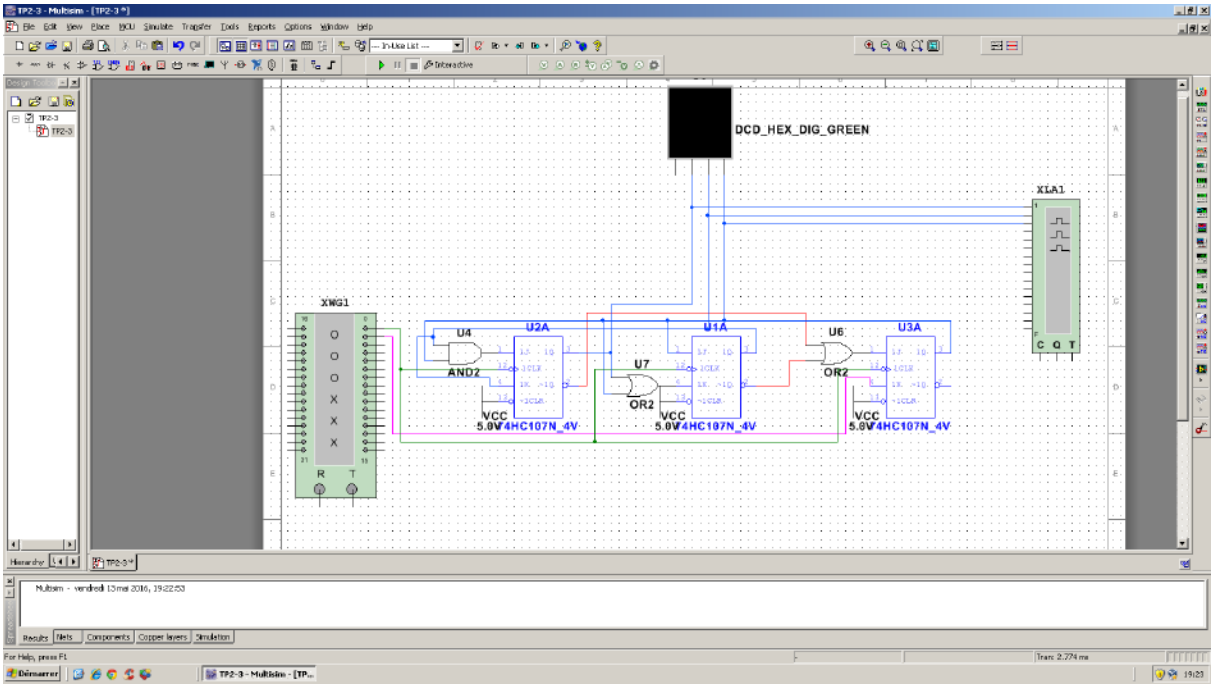

TP2-2 - Multisim - [TP2-2 *]
U5
DCD_HEX_DIG_GREEN
XWG1
XLA1
VCC
5.0V
U1A
U2A
U3A
74HC74D_4V
U11
AND3
U12
AND2
U13
OR2
U7
AND2
U8
AND2
U4
AND2
U5
AND2
U10
OR2
U9
OR2

2.3)

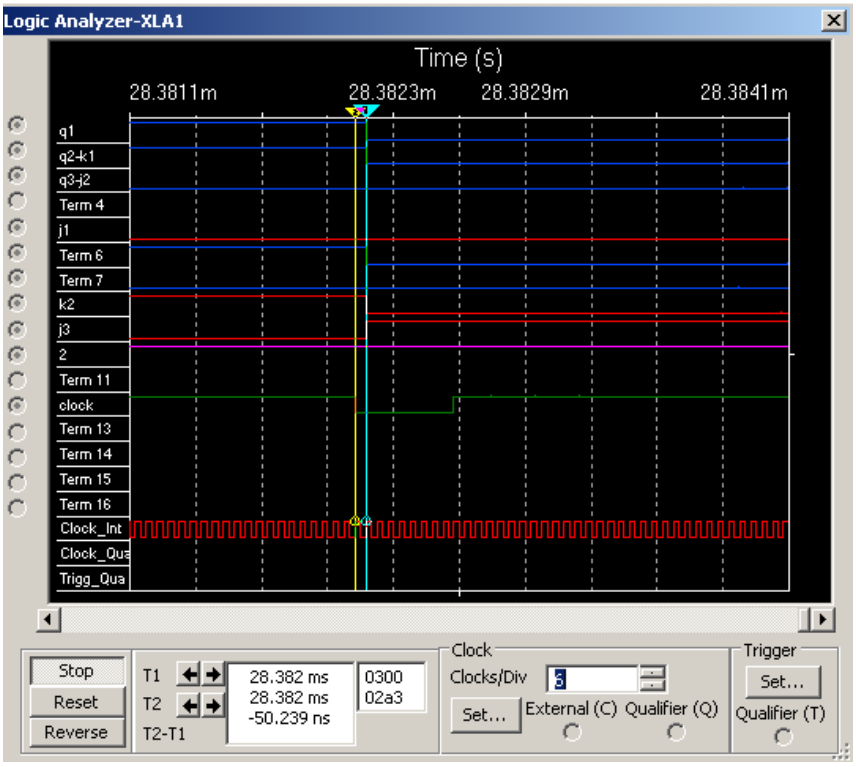



Logic Analyzer-XLA1
Time (s)
244.000µ 245.500µ 247.000µ 248.500µ 250.000µ 251.500µ
q1
q2
q3
Term 4
da
db
dc
Term 8
clock
Term 10
Term 11
Term 12
Term 13
Term 14
Term 15
Term 16
Clock_Int
Clock_Qua
Trigg_Qua
Stop
Reset
Reverse
T1
T2
T2-T1
0000
0000
Clock
Clocks/Div
15
Set...
External (C)
Qualifier (Q)
Trigger
Set...
Qualifier (T)

3.2)



3.3)



Dans l'ordre :

q1, q2, q3, j1, k1, j2, k2, j3, k3, clock.