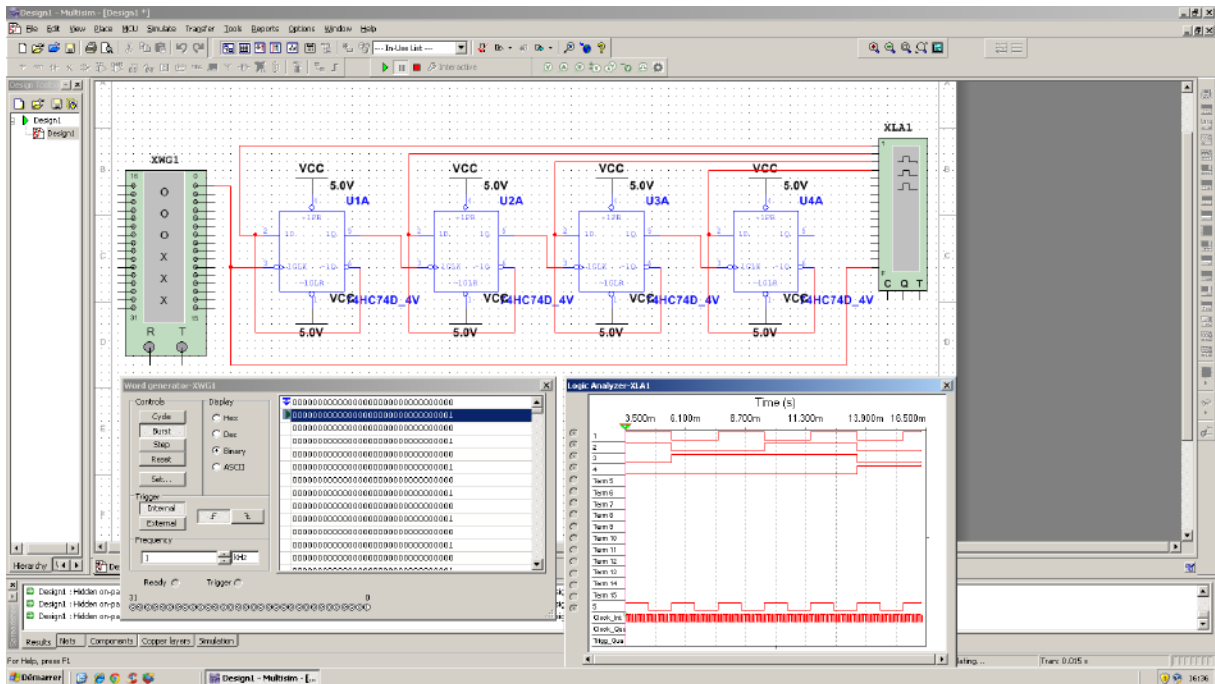
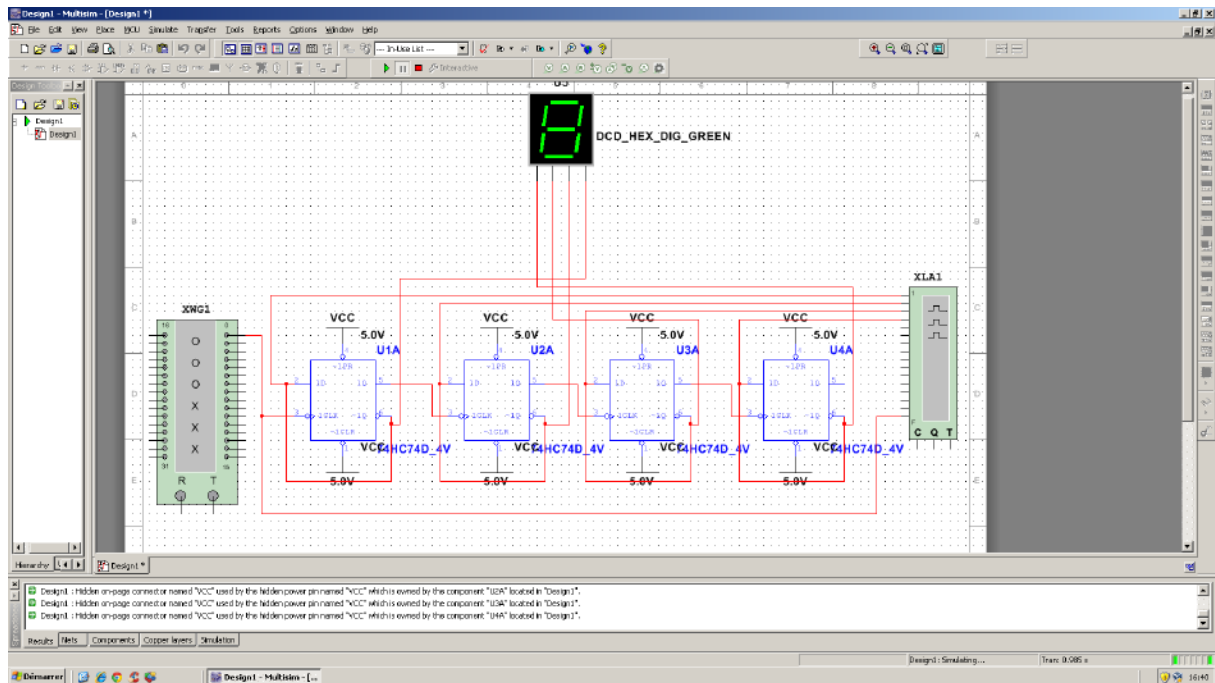


1.2)



Avec afficheur:



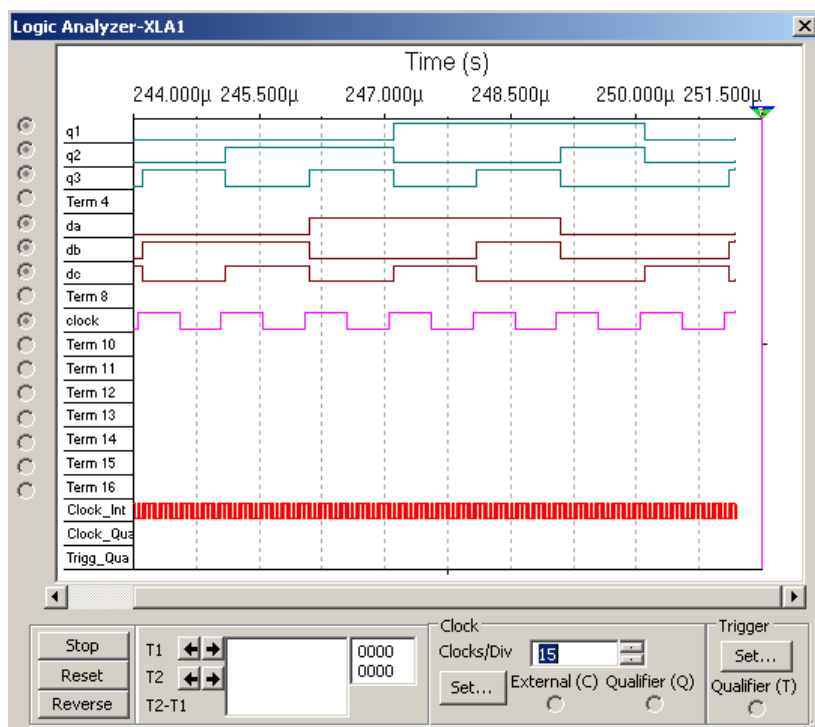
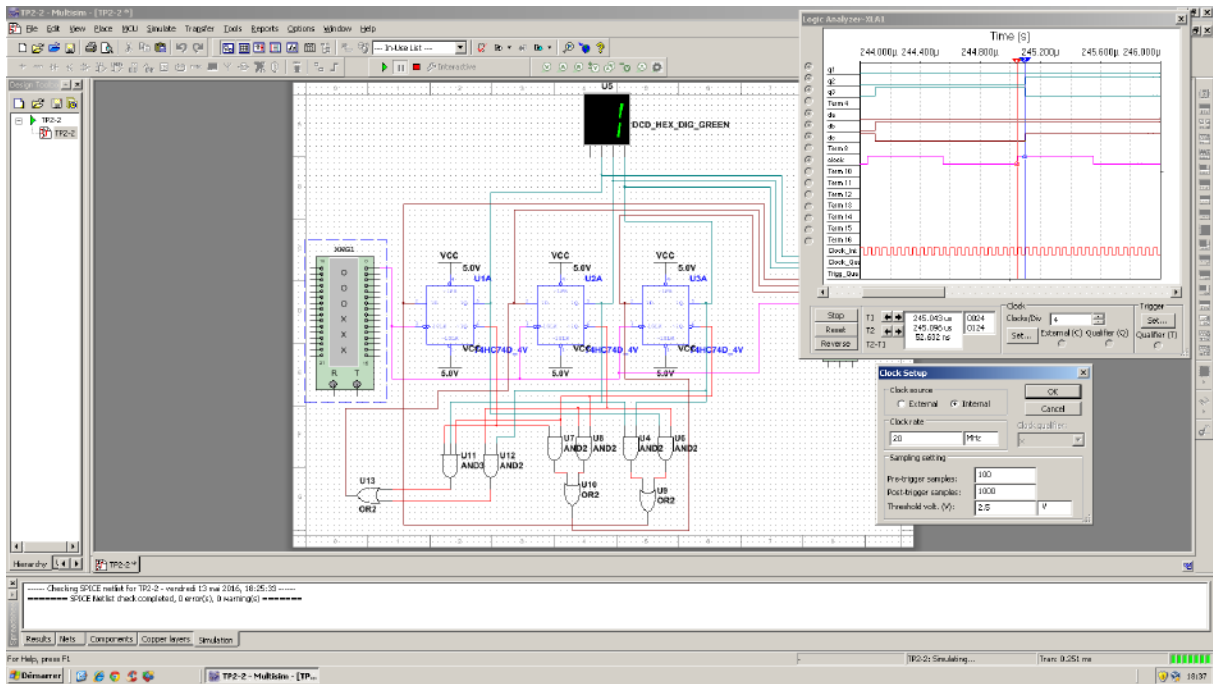
1.3)

The screenshot displays a digital logic simulation environment. On the left, a timing diagram shows a clock signal (red) and a data signal (blue) over a 500ns period. The circuit schematic in the center shows four 7448 BCD-to-7-segment decoders (U1A-U1D) connected to a 7-segment display (US1) showing the digit '1'. A 'Word generator' window on the right displays a sequence of hexadecimal values. A 'Clock Setup' dialog box is open in the foreground, showing settings for clock source, rate, and sampling.

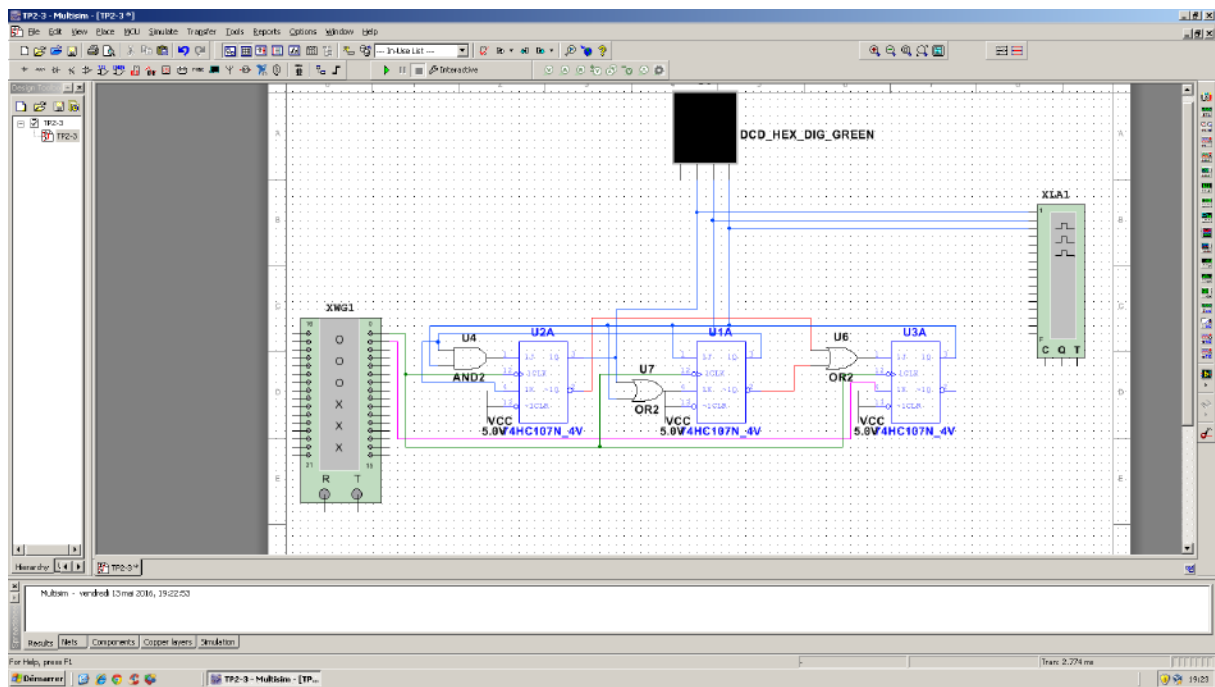
2.2)

The screenshot displays a digital logic simulation environment. The circuit schematic features a 7448 BCD-to-7-segment decoder (U1A) connected to a 7-segment display (US1) showing the digit '2'. The circuit includes several logic gates (AND, OR) and a Schmitt trigger (U13). The schematic is more complex than in the previous image, with multiple logic gates and a Schmitt trigger.

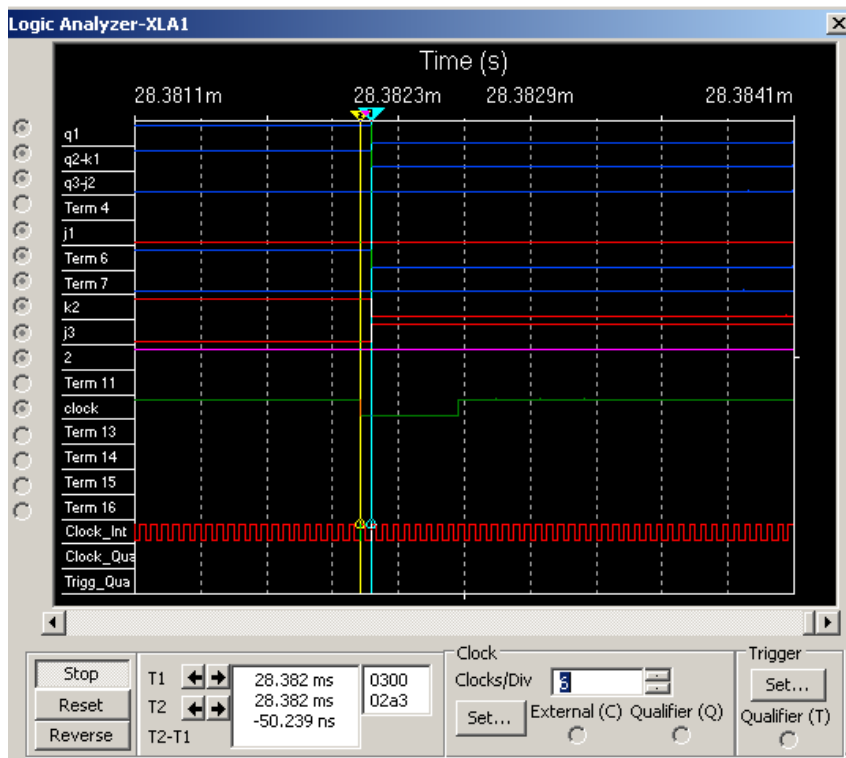
2.3)



3.2)



3.3)



Dans l'ordre :

q1, q2, q3, j1, k1, j2, k2, j3, k3, clock.