

ADD #1, D0

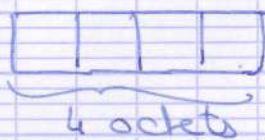
SUB #1, D1

BNE -7 (continue de BRZ (Branch if Not Equal))

Architecture générale Processeurs / Mémoire.

Exercice 1.

mot mémoire :



Cache mémoire

ex 3.

1 bus synchrone $\Rightarrow$ 4 cycles pour lire un mot

2.

$$\begin{aligned} D &= \frac{F \cdot N}{c} = \frac{10^7 \times 16}{4} = 4 \times 10^7 \text{ bits/s} \\ &= 40 \text{ Mbits/s} \xrightarrow{\text{FPI. de bit}} \\ &= 5 \times 10^6 \text{ octets} = 5 \text{ Mo/s.} \end{aligned}$$

ex 4

1. $640 \times 480 = 307200$ pixel / image.

$307200 \times 4 \times 50 = 60 \text{ Mbits/s}$

$307200 \times 4 \times 60 = 72 \text{ Mbits/s}$

$$\begin{aligned}
 2. \quad \alpha &\approx 1 \times 25 = 1,5 \times 1024^{x8 \times 1024} \text{ bits/s.} \\
 25\alpha &= 12 \text{ n bit/s.} \\
 \alpha &= \frac{12 \times 1024 \times 1024}{25} = 503316,48.
 \end{aligned}$$

$$12 \alpha^2 = 503316,48.$$

$$\alpha = \sqrt{\frac{503316,48}{12}}$$

$$\alpha = 204,8.$$

$$\begin{aligned}
 819,2 \times 614,4 \\
 \approx 800 \times 600
 \end{aligned}$$



exc 5.

lecture memoire via un bus asynchrone.

